Attorney Docket No. SAM-126
PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, D.C. 20231

NEW APPLICATION TRANSMITTAL

Transmitted herewith for filing is the patent application of

Inventor(s): In-Jung Lee and Heon -Juong Shin

For (title): CAPACITOR AND FABRICATION METHOD THEREFOR

CERTIFICATE OF MAILING
37 C.F.R. § 1.10
"Express Mail" Mailing Label Number EL562433084US
I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated above and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

Date aug 7, 2000 Vanessa Marakas
Vanessa Marakas
Vanessa Marakas
Print Name

1. **Type of Application** This new application is for a(n)

☒ Original (nonprovisional)
☐ Design
☐ Plant
☐ Divisional.
☐ Continuation.
☐ Continuation-in-part (C-I-P).

2. **Benefit of Prior Application(s)**

☒ The new application being transmitted claims the benefit of prior Korean application(s) nos. 2000-00280. See item 7 .

3. **Papers Enclosed**

10 Pages of specification

3 Pages of claims

1 Page of Abstract

4 Sheets of drawings
☐ formal
☒ informal

_____ Page of Cover Sheet

☐ The **enclosed** drawing(s) are photograph(s), and there is also attached a "PETITION TO ACCEPT PHOTOGRAPH(S) AS DRAWING(S)." 37 C.F.R. 1.84(b).

4. Additional papers enclosed

- ☐ Preliminary Amendment
- ☐ Information Disclosure Statement (37 C.F.R. 1.98)
- ☐ Form PTO-1449 (PTO/SB/08A and 08B)
- ☐ Copies of cited references
- ☐ Declaration of Biological Deposit
- ☐ Submission of "Sequence Listing," computer readable copy and/or amendment pertaining thereto for biotechnology invention containing nucleoticle and/or amino acid sequence.
- ☐ Authorization of Attorney(s) to Accept and Follow Instructions from Representative
- ☐ Special Comments
- ☒ Other: Return Postcard.

5. Declaration or oath

- ☒ Enclosed
  - ☐ Unexecuted
  - ☒ Executed by
    - ☒ inventors
    - ☐ legal representative of inventor(s). 37 CFR 1.42 or 1.43.
    - ☐ joint inventor or person showing a proprietary interest on behalf of inventor who refused to sign or cannot be reached.
    - ☐ This is the petition required by 37 CFR 1.47 and the statement required by 37 CFR 1.47 is also attached. See item 12 below for fee.
- ☐ Not Enclosed

☐ Application is made by a person authorized under 37 C.F.R. 1.41 (c) on behalf of all the above named inventor(s).

- ☐ Showing that the filing is authorized.

6. Assignment

☒ An assignment of the invention to Samsung Electronics Co., Ltd.

☒ is attached. A separate ☐ "COVER SHEET FOR ASSIGNMENT (DOCUMENT) ACCOMPANYING NEW PATENT APPLICATION" or ☒FORM PTO 1595 is also attached.

☐ will follow.

7. **Certified Copy**

Certified copy(ies) of application(s)

Korea	2000-00280	05 January 2000
Country	Appln. no.	Filed
Country	Appln. no.	Filed
Country	Appln. no.	Filed

from which priority is claimed

☒ is (are) attached.

☐ will follow.

8. **Fee Calculation (37 C.F.R. 1.16)**

CLAIMS AS FILED

	Number filed		Number Extra	Rate
Basic Fee				37 C.F.R. 1.16(a) $690.00
Total Claims (37 CFR 1.16(c))	13	- 20 =	0	$ 18.00
Independent Claims (37 CFR 1.16(b))	1	- 3 =	0	$ 78.00
Multiple dependent claim(s), if any (37 CFR 1.16(d))			+	$260.00

☐ A Preliminary Amendment canceling claims is enclosed. The filing fee is calculated based on the number of claims remaining after entry of the Preliminary Amendment.

☐ Amendment deleting multiple-dependencies is enclosed.

☐ Fee for extra claims is not being paid at this time.

Filing Fee Calculation $ 690.00

9. Small Entity Statement(s)

☐ Verified Statement(s) that this is a filing by a small entity under 37 CFR 1.9 and 1.27 is (are) attached.

☐ Status as a small entity was claimed in prior application _____, filed on_____ from which benefit is being claimed for this application under:

35 U.S.C. ☐ 119(e),

☐ 120,

☐ 121,

☐ 365(c),

and which status as a small entity is still proper and desired.

☐ A copy of the verified statement in the prior application is included.

Filing Fee Calculation (50% of A, B or C above)

$_____

10. Fee Payment Being Made at This Time

☐ Not Enclosed

☐ No filing fee is to be paid at this time.
(This and the surcharge required by 3 7 C. F.R. 1.16(e) can be paid subsequently.)

☒ Enclosed

☒ Basic filing fee $ 690.00

☒ Recording assignment
($40.00; 37 C.F.R. 1.21(h))
(See attached "COVER SHEET FOR ASSIGNMENT ACCOMPANYING NEW APPLICATION".) $ 40.00

Total fees enclosed **$ 730.00**

11. Method of Payment of Fees

☒ Checks in the amounts of $ 690.00, 40.00

☐ Charge Account No. 19-0079 in the amount of $ _____
A duplicate of this transmittal is attached.

12. Authorization to Charge Additional Fees

☒ The Commissioner is hereby authorized to charge the following additional fees during the entire pendency of this application to Account No. 19-0079.

- ☒ 37 C.F.R. 1.16(a), (f) or (g) (filing fees)
- ☒ 37 C.F.R. 1.16(b), (c) and (d) (presentation of extra claims)
- ☐ 37 C.F.R. 1. 1 6(e) (surcharge for filing the basic filing fee and/or declaration on a date later than the filing date of the application)
- ☐ 37 C.F.R. 1.17 (application processing fees)
- ☐ 37 C.F.R. 1.18 (issue fee at or before mailing of Notice of Allowance, pursuant to 37 C.F.R. 1.311(b))

13. Instructions as to Overpayment

- ☒ Credit Account No. 19-0079
- ☐ Refund

Respectfully submitted,

Date: August 7, 2000

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

Samuels, Gauthier & Stevens, LLP
225 Franklin Street, Suite 3300
Boston, MA 02110
Telephone: (617) 426-9180, Ext. 148
Facsimile: (617) 426-2275

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08-08-00

PATENT
Attorney Docket No. SAM-126

A

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Applicant(s): In-Jung Lee and Heon-Joung Shin
Filing Date: Herewith
Title: CAPACITOR AND FABRICATION METHOD THEREFOR

CERTIFICATE OF MAILING UNDER 37 C.F.R.§ 1.10

"Express Mail" Mailing Label Number EL562433084US I hereby certify that this paper or fee is being deposited with the United States Postal Service "Express Mail Post Office to Addressee" service under 37 CFR 1.10 on the date indicated below and is addressed to BOX PATENT APPLICATION, Assistant Commissioner for Patents, Washington, DC 20231.

August 7, 2000
Date

Vanessa Marakas
Vanessa Marakas

BOX PATENT APPLICATION
Assistant Commissioner for Patents
Washington, DC 20231

TRANSMITTAL LETTER

Sir:

Enclosed herewith for filing in the above-identified patent application please find the following listed items:

1. New Application Transmittal;
2. New Patent Application;
3. Executed Declaration, Petition and Power of Attorney;
4. Four (4) Sheets of Informal Drawings;
5. Certified Copy of Priority Document - Korean Application No 2000-00280;
6. Check in the amount of $690.00 to cover requisite fee;
7. Assignment Recordation Form Cover Sheet - - PTO-1595;
8. Executed Assignment;
9. Check in the amount of $40.00 to cover assignment recordation fee; and
10. Return Postcard.

In connection with the foregoing matter, please charge any additional fees which may be due, or credit any overpayment, to Deposit Account Number 19-0079. A duplicate copy of this letter is provided for this purpose.

Respectfully submitted,

Date: August 7, 2000

Samuels, Gauthier & Stevens, LLP
225 Franklin Street, Suite 3300
Boston, MA 02110
Telephone: (617) 426-9180, Ext. 148
Facsimile: (617) 426-2275

Anthony P. Onello, Jr.
Registration Number 38,572
Attorney for Applicant

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CAPACITOR AND FABRICATING METHOD THEREFOR

BACKGROUND OF THE INVENTION

FIELD OF THE INVENTION

The present invention relates to a semiconductor device and a fabricating method therefor, and more particularly to a capacitor and a fabricating method therefor in an manner that prevents the occurrence of lifting between a polysilicon pattern and a blocking metal layer of an upper electrode in the process of a wire-bond attached chip capacitor (hereinafter referred to as WACC).

DESCRIPTION OF THE PRIOR ART

A wire-bond attached chip capacitor (WACC) is mounted to an integrated circuit (IC), or chip, for enhancement of stable operation. The WACC is coupled to the IC by wire-bonding pads respectively positioned between the IC components and the WACC.

Generally, the WACC has been widely deployed in the power supply of semiconductor devices and other electronic devices. Figs. 1a through 1d are diagrams for illustrating sequential processes of a conventional WACC fabrication method. With reference to the drawings, the method for fabricating the conventional WACC will now be described in detail.

As shown in Fig. 1a, a first insulating layer 12 of an oxide layer is formed on a p++ type silicon substrate 10. The first insulating layer 12 is selectively etched to expose an active area of the substrate 10. Accordingly, the substrate 10 of the active area positioned at the upper electrode is selectively etched to a predetermined thickness to form a plurality of trenches (t) in the substrate 10.

As shown in Fig. 1b, an oxide-nitride-oxide (ONO) dielectric layer 14 is formed on the resultant structure of Fig. 1a. A polysilicon layer 16 is constructed in a deposition structure comprising an undoped polysilicon layer 16a below a doped polysilicon layer 16b (referred to herein as an "undoped/doped" structure) formed over the dielectric layer 14. At this time, the undoped polysilicon layer 16a is formed at a thickness of 500 Angstroms (hereinafter referred to as A) at 620 °C, while the doped polysilicon layer 16b is formed at a thickness of 2500A at 540 °C. The purpose of the 'undoped/doped' doubly layered structure in the polysilicon layer 16 is because the trenches t are formed for fabricating a capacitor to increase its effective area in designing a semiconductor device in accordance with a design rule of less than 0.25μm. Relying on solely the application of a general impurity impregnation process, it would be difficult to impregnate enough impurity to the upper end of the polysilicon layer 16.

As shown in Fig. 1c, the polysilicon layer 16 is removed, save the region of the upper electrode forming portion, so as to form a polysilicon pattern 16'. In the aforementioned process, the top oxide layer of the ONO dielectric layer 14 is also removed, causing thinning of the resultant dielectric layer 14. Accordingly, any remaining dielectric layer 14 remaining beyond the portion covered by the polysilicon pattern 16' is eliminated. In order to make an ohmic contact between a blocking metal layer (a layer to be deposited during the next step) and the active area, p+ type impurity 24 is ion-impregnated in blanket onto the structure. As a result, a p+ type impurity diffusion area 18 is formed in the substrate 10 in the active region positioned at one side of the polysilicon pattern 16'.

As shown in Fig. 1d, the blocking metal layer is formed and annealed over the surface constructed by the previous processes, and an aluminum layer is, then, formed thereon. As a result, a first metal layer of a "blocking metal layer / aluminum layer" deposition structure is formed. For

example, the blocking layer may comprise a "Ti/TiN" deposition structure, wherein Ti is formed in thickness of 150A and TiN is formed in thickness of 1000A. The Ti of the blocking metal layer forms a silicide layer by reacting with the lower silicon (named for the combination of the polysilicon pattern and p++ type silicon substrate) in the annealing process, so as to improve adhesion between the blocking metal layer and silicon. TiN of the blocking metal layer prevents diffusion of the aluminum layer into the silicon in the deposition of the first metal layer. Accordingly, the first metal layer is selectively etched to expose a predetermined part of the first insulating layer 12, thereby respectively forming a first metal pattern 20a to be connected with the polysilicon pattern 16' and a first metal pattern 20b to be connected with the p+ type impurity diffusion area 18. Then, a second insulating layer 22 made of an oxide layer as inter-layer insulating material is formed on the first insulating layer 12 that includes the first metal patterns 20a, 20b. A via hole (h) is then formed by selectively etching the second insulating layer 22 to expose a predetermined portion of the first metal pattern 20b connected with the p+ type impurity diffusion area 18. Finally, the second metal pattern 24 is formed on the second insulating layer 22 that includes the via hole (h), thereby completing the fabrication process.

As shown in Fig. 1d, a WACC is thus fabricated in the structure having an upper electrode (I) on its top portion, in which the polysilicon pattern 16' and the first metal pattern 20a are connected with the dielectric layer 14 positioned therebetween, and a lower electrode (II) on its bottom portion, in which the first metal pattern 20b and the second metal pattern 24 are connected with the p++ type substrate 10.

As a consequence of the above process, however, the fabricated WACC suffers from a number of limitations. For example, adhesion between the silicon and the upper blocking metal layer is determined by the degree to which the Ti and silicon react during the annealing process.

The thickness of the resultant layer (for example the silicide layer) is generally known to be inversely proportional to the doping level of the lower silicon layer. In other words, if the impurity doping level of the lower silicon is high, the reacted layer becomes thinner. If the impurity doping level of the lower silicon is low, the reacted layer becomes thicker. In this configuration, the lower silicon layer indicates all of the polysilicon pattern 16' and the p++ type substrate 10.

Thus, in order to improve adhesion between Ti and silicon, the thickness of the reacted layer should be higher than a predetermined level thereof by lowering the impurity doping level of the lower silicon.

However, when the WACC is fabricated according to the aforementioned processes, the polysilicon layer is constructed in the "undoped/doped" double deposition structure. As a result, in addition to the high doping level of the polysilicon layer, the impurity doping level of the polysilicon pattern 16' becomes much higher by the blanket ion-impregnation of p+ type impurity, which has been additionally formed to make an ohmic contact. For this reason, the silicide layer is marginally formed between the polysilicon pattern 16' and the blocking metal layer. As a consequence, a problem arises in that adhesion between the polysilicon pattern 16' and the blocking metal layer of the upper electrode becomes weak, thereby resulting in the phenomenon of lifting therebetween.

SUMMARY OF THE INVENTION

It is therefore an object of the present invention to address the aforementioned limitations by providing a WACC having an upper electrode with its polysilicon layer constructed in a triply-layered deposition structure of "undoped/ doped/ undoped polysilicon layers" to enable the polysilicon layer contacting the blocking metal layer to be the undoped polysilicon layer. In

this manner, an effective silicide layer is formed between the polysilicon layer and the blocking metal layer to reinforce adhesion and prevent occurrence of lifting therebetween.

It is another object of the present invention to provide a method for fabricating a capacitor that helps to effectively produce the semiconductor device constructed in the aforementioned structure.

In order to accomplish the aforementioned object of the present invention, there is provided a capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode is constructed in a deposition structure of "first undoped polysilicon layer/ doped polysilicon layer/ second polysilicon layer".

In order to accomplish the other object of the present invention, there is provided a method for fabricating a capacitor having lower electrode, dielectric layer and upper electrode, wherein the upper electrode is formed in a deposition structure comprising a "first undoped polysilicon layer/ doped polysilicon layer/ second undoped polysilicon layer".

It is preferred that the first and second undoped polysilicon layers be formed at a thickness of less than 1000A, the doped polysilicon layer be formed in thickness of 1800-2500A, and the second undoped polysilicon layer be formed under the same temperature as that of the doped layer without any breakup of vacuum after formation of the doped polysilicon layer.

It is further preferred that the capacitor be designed to have a metal pattern in a deposition structure comprising "blocking metal layer/ aluminum layer". The blocking metal layer is preferably constructed in a "Ti/TiN" deposition structure.

In the WACC thus fabricated, the blocking metal layer is contacted with an undoped polysilicon layer, rather than a doped polysilicon layer as in the conventional embodiment, to achieve the effect of reducing the doffing level of the polysilicon layer to lower than that of the

conventional embodiment. This configuration significantly improves effectiveness in formation of a silicide layer between the polysilicon layer and the blocking metal layer, and prevents the occurrence of lifting therein.

BRIEF DESCRIPTION OF THE DRAWINGS

The foregoing and other objects, features and advantages of the invention will be apparent from the more particular description of preferred embodiments of the invention, as illustrated in the accompanying drawings in which like reference characters refer to the same parts throughout the different views. The drawings are not necessarily to scale, emphasis instead being placed upon illustrating the principles of the invention.

Figs. 1a through 1d are diagrams for illustrating sequential processes for a conventional WACC fabrication method.

Figs. 2a through 2d are diagrams for illustrating sequential processes for a WACC fabrication method according to the present invention.

DETAILED DESCRIPTION OF PREFERRED EMBODIMENTS

Objects and aspects of the present invention will become apparent from the following detailed description of preferred embodiments with reference to the accompanying drawings.

Figs. 2a through 2d are diagrams for illustrating sequential processes for a WACC fabricating method of the present invention. With reference to the aforementioned drawings, the sequential processes for fabricating WACC will be described below.

As shown in Fig. 2a, a first insulating layer 102 of an oxide layer is formed on a p++ type silicon substrate 100, and the first insulating layer 102 is selectively etched to expose active

regions 126 of the substrate. Accordingly, the substrate 100 in the active regions positioned at an upper electrode portion is selectively etched at a predetermined thickness to form a plurality of trenches (t) in the substrate 100.

As shown in Fig. 2b, an oxide-nitride-oxide (ONO) dielectric layer 104 is formed on the resultant structure of Fig. 2a. In order to sufficiently fill up the trenches t, a polysilicon layer 106 is constructed according to the following deposition structure of a "first undoped polysilicon layer 106a/ doped polysilicon layer 106b/ second undoped polysilicon layer 106c" on the dielectric layer 104. The first undoped polysilicon layer 106a is preferably formed at a thickness of 1000A at 620 °C, while the doped polysilicon layer 106b is formed at a thickness of 1800A - 2500A at 540 °C. The second undoped polysilicon layer 106c is formed at a thickness of 1000A at 540 °C without any breakup of vacuum after formation of the doped polysilicon layer 106b. The polysilicon layer 106 is constructed in this triply-layered deposition structure of "first undoped/ doped/ second undoped polysilicon" layers because it is preferred that the polysilicon layer in contact with the Ti of the blocking metal layer is the undoped form polysilicon layer during the deposition process of the following blocking metal layer (for instance, a "Ti/TiN" deposition structure of the blocking metal layer). In this manner, the doffing level of the polysilicon layer in contact with the blocking metal layer is lower for the configuration of the present invention as compared to that of the conventional configuration.

As shown in Fig. 2c, the polysilicon layer 106, save the region of the electrode, is removed to form a polysilicon pattern 106'. According to the aforementioned process, the top oxide layer of the ONO dielectric layer 104 is also removed, causing thinning of the resultant dielectric layer 104 during completion of the etching process. Accordingly, the remaining portion of the dielectric layer 104 is eliminated. In order to make an ohmic contact between the blocking

metal layer to be deposited during the following step and the active region, p+ type impurity is ion-impregnated in blanket onto the formed structure. As a result, the p+ type impurity diffusion region 108 is formed in the substrate 100 in the active region 126.

As shown in Fig. 2d, the blocking metal layer is formed and annealed over the surface constructed by the previous process, and an aluminum layer is then formed thereon. As a result, a first metal layer of a "blocking metal layer/ aluminum layer" deposition structure is formed. The blocking metal layer preferably comprises a "Ti/TiN" deposition structure, wherein Ti is formed at a thickness of 150A and TiN is formed at a thickness of 1000A. The Ti of the blocking metal layer forms a silicide layer during the annealing process by reacting with silicon (named for all of the polysilicon pattern and p++ type silicon substrate), so as to improve adhesion between the blocking metal layer and silicon. Further, the TiN of the blocking metal layer prevents diffusion of the aluminum layer into the silicon during deposition of the first metal layer. Accordingly, the first metal layer 110 is selectively etched to expose a predetermined part of the first insulating layer 102, thereby respectively forming a first metal pattern 110a to be connected with the polysilicon pattern 106' and a first metal pattern 110b to be connected with the p+ type impurity diffusion area 108. Next, a second insulating layer 112 comprising an oxide layer as inter-layer insulating material is formed on the first insulating layer 102 and the first metal patterns 110a, 110b, and a via hole is formed by selectively etching the second insulating layer 112 to expose a predetermined part of the first metal pattern 110b connected with the p+ type impurity diffusion area 108. Finally, the second metal pattern 114 is formed on the second insulating layer 112 including the via hole, thereby completing the fabrication process.

As shown in Fig. 2d, a WACC is completed in a structure having an upper electrode (I) on its top portion, in which the polysilicon pattern 106' and the first metal pattern 110a are

connected above the substrate 100, with the dielectric layer 104 being positioned therebetween, and the lower electrode (II) on its bottom portion, in which the first and second metal pattern 110b, 114 are connected with the p++ type substrate 100.

As described above, the polysilicon pattern 106' is constructed in a triply layered deposition structure of "first undoped polysilicon layer 106a/ doped polysilicon layer 106b/ second undoped polysilicon layer 106c", while the first metal patterns 110a, 110b are constructed in the "blocking metal layer/ aluminum layer" deposition structure.

In the case of a WACC thus constructed, the Ti of the blocking metal layer contacts the second undoped polysilicon layer 106c to achieve an effect that the doffing level of the polysilicon layer is lower for the configuration of the present invention as compared to that of the conventional configuration, so that the silicide layer is more readily formed between the polysilicon layer and the blocking metal layer.

As a result, the structure of the WACC thus constructed provides enhancement of adhesion between polysilicon pattern 106' and blocking metal layer, and prevention and/or mitigation of the occurrence of lifting between the blocking metal layer and the polysilicon pattern 106' of the upper electrode.

As described above, there is an advantage in the WACC of the present invention, in that the polysilicon layer of the upper electrode is constructed in the triply layered deposition structure of "undoped/ doped/ undoped" to enable the undoped polysilicon layer come in contact with the blocking metal layer, thereby enhancing formation of a silicide layer between the polysilicon layer and the blocking metal layer (particularly, Ti) to improve adhesion and prevent the occurrence of lifting.

While this invention has been particularly shown and described with reference to preferred embodiments thereof, it will be understood by those skilled in the art that various changes in form and detail may be made herein without departing from the spirit and scope of the invention as defined by the appended claims.

CLAIMS

What is claimed is:

1. A semiconductor capacitor having a lower electrode, a dielectric layer and an upper electrode, wherein the upper electrode comprises a deposition structure including a doped polysilicon layer formed between a first undoped polysilicon layer and a second undoped polysilicon layer.

2. The capacitor, as defined in claim 1, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.

3. The capacitor, as defined in claim 1, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.

4. The capacitor, as defined in claim 1, wherein an additional metal pattern is deposited over the upper electrode.

5. The capacitor, as defined in claim 4, wherein the metal pattern is constructed in a deposition structure including a blocking metal layer and an aluminum layer.

6. The capacitor, as defined in claim 5, wherein the blocking metal layer is constructed in a structure including a Ti layer and a TiN layer.

7. A method for fabricating a capacitor having a lower electrode, a dielectric layer and upper electrode, wherein the upper electrode is formed according to the following steps:

forming a first undoped polysilicon layer;

forming a doped polysilicon layer on the first undoped polysilicon layer; and

forming a second undoped polysilicon layer on the doped polysilicon layer.

8. The method, as defined in claim 7, wherein the first and second undoped polysilicon layers are formed at a thickness of less than 1000A.

9. The method, as defined in claim 7, wherein the doped polysilicon layer is formed at a thickness between 1800A and 2500A.

10. The method, as defined in claim 7, wherein the second undoped polysilicon layer is formed at the same temperature as that of the doped layer without any breakup of vacuum following formation of the doped polysilicon layer.

11. The method, as defined in claim 7, wherein an additional metal pattern is deposited over the upper electrode.

12. The method, as defined in claim 11, wherein the metal pattern is constructed in a deposition structure including a blocking metal layer and an aluminum layer.

13. The method, as defined in claim 12, wherein the blocking metal layer is constructed in a structure including a Ti layer and a TiN layer.

CAPACITOR AND FABRICATING METHOD THEREFOR

ABSTRACT OF THE DISCLOSURE

The present invention relates to a WACC and a fabricating method thereof to prevent the occurrence of lifting between a polysilicon layer pattern and blocking metal layer of an upper electrode. In order to accomplish the object of the present invention, there is provided a capacitor having upper and lower electrodes and a dielectric layer therebetween, wherein the upper electrode has a polysilicon pattern constructed in a deposition structure of "first undoped polysilicon layer/ doped polysilicon layer/ second undoped polysilicon layer" to be connected with a first metal pattern at the top portion, and the lower electrode has first and second metal patterns to be connected with a p++ type silicon substrate at the bottom portion. The first metal pattern is preferably constructed in a deposition structure of "blocking metal layer/ aluminum layer", where the blocking metal layer is preferably constructed in a "Ti/TiN" deposition structure. Accordingly, the capacitor is constructed to enable the blocking metal layer to be in contact with an undoped polysilicon layer, rather than a doped polysilicon layer as in conventional embodiments, to achieve an effect that the doffing level of the polysilicon layer is reduced as compared to the conventional configuration, thereby enhancing formation of the silicide layer between the polysilicon layer and the blocking metal layer to improve adhesion and prevent the occurrence of lifting.

Fig. 1a (PRIOR ART)

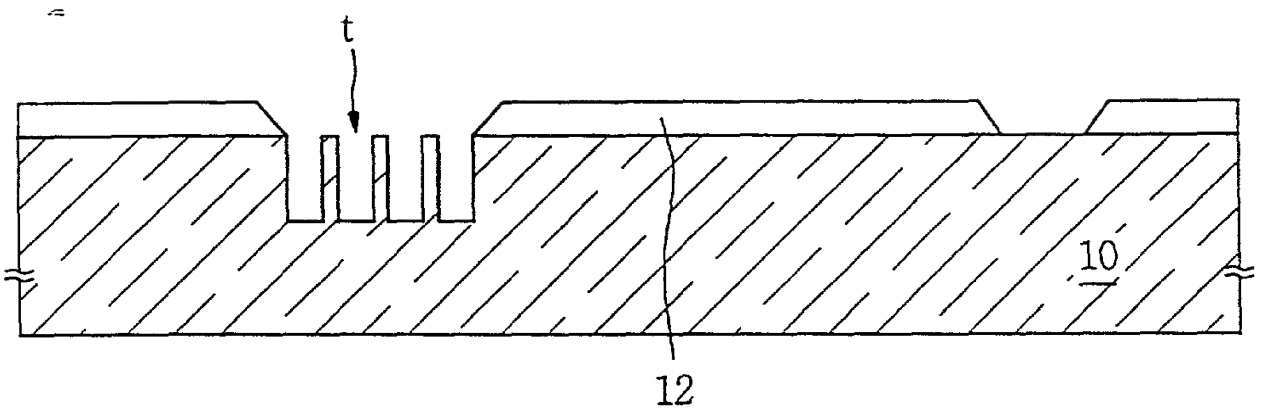


Fig. 1b (PRIOR ART)

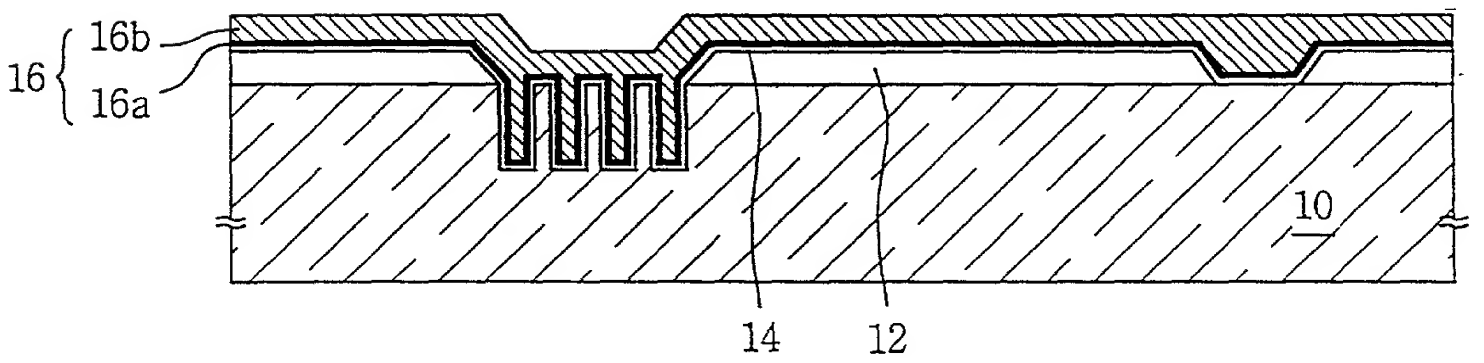


Fig. 1c (PRIOR ART)

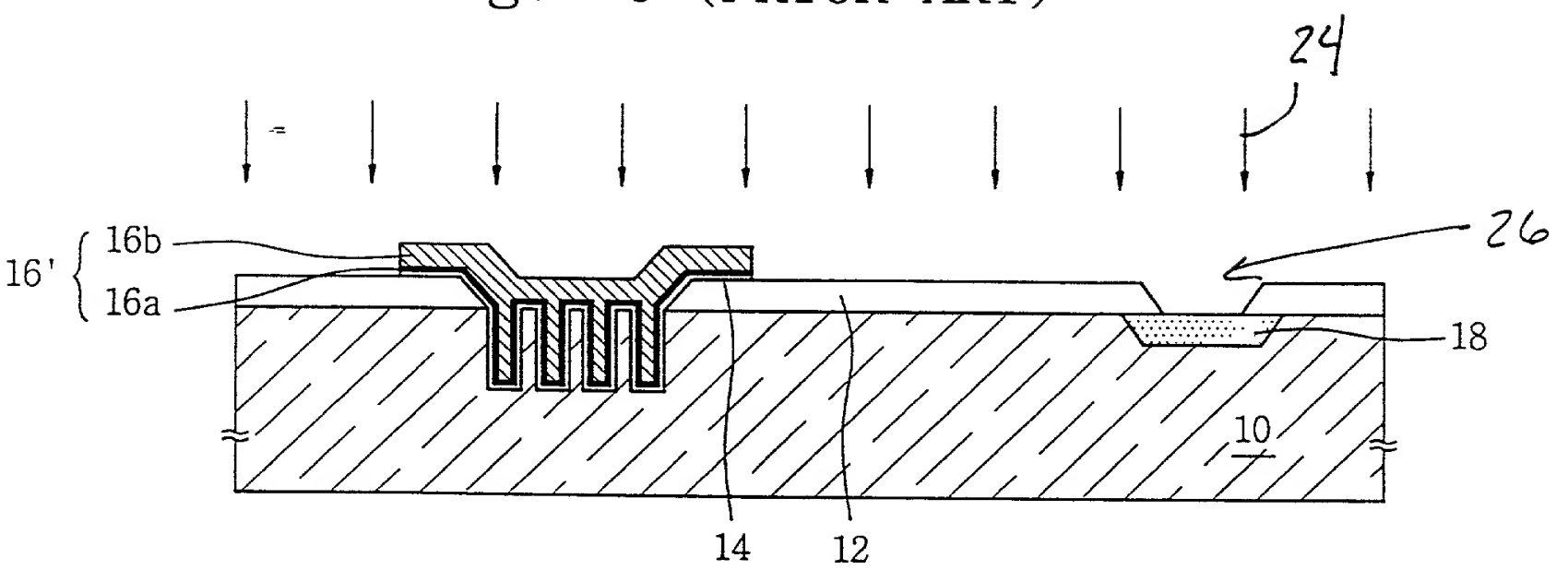


Fig. 1d (PRIOR ART)

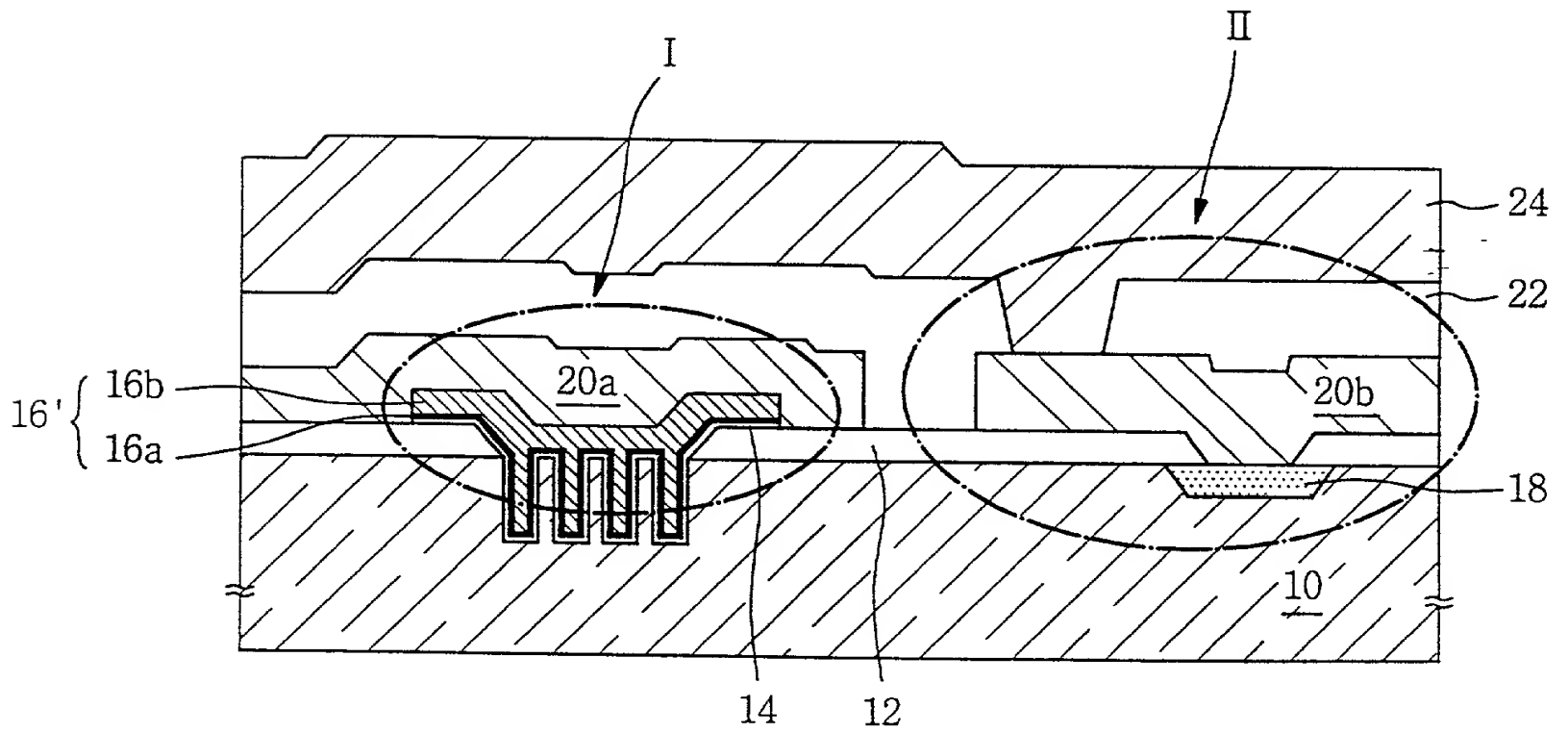


Fig. 2a

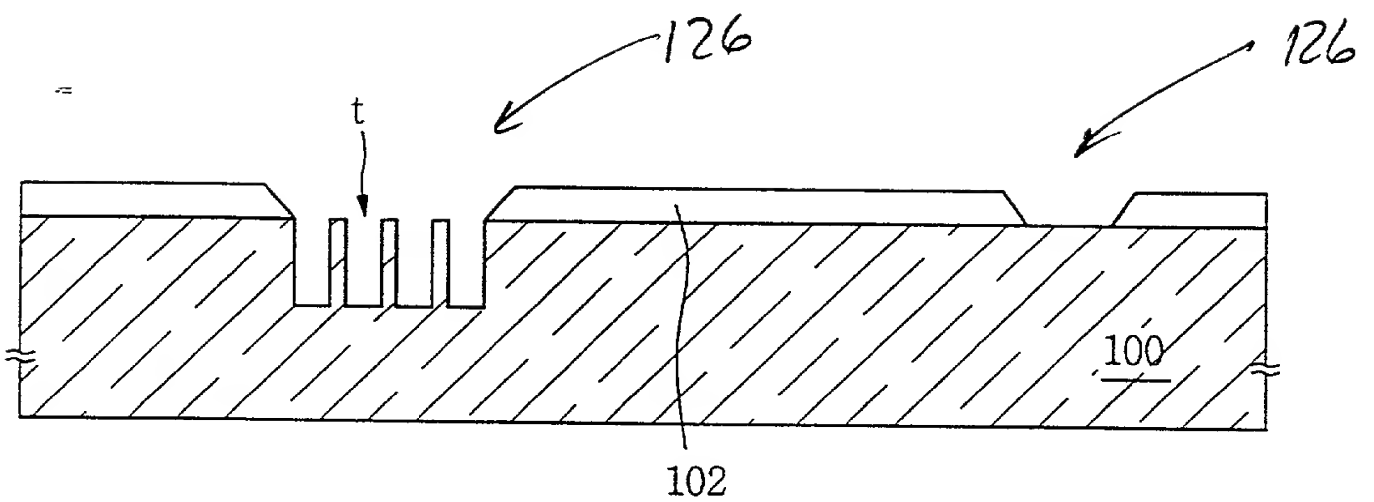


Fig. 2b

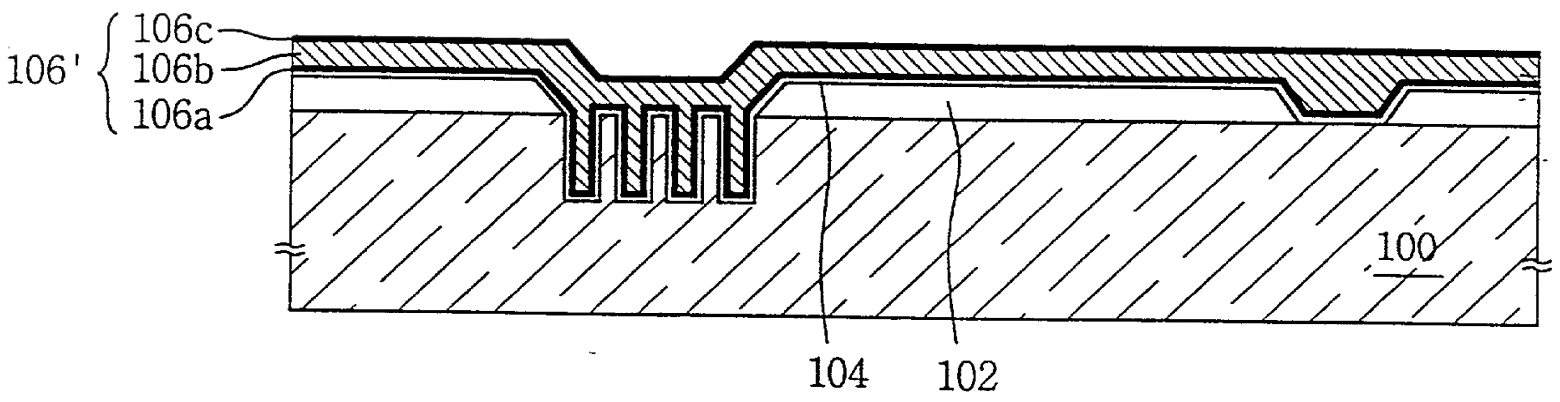


Fig. 2c

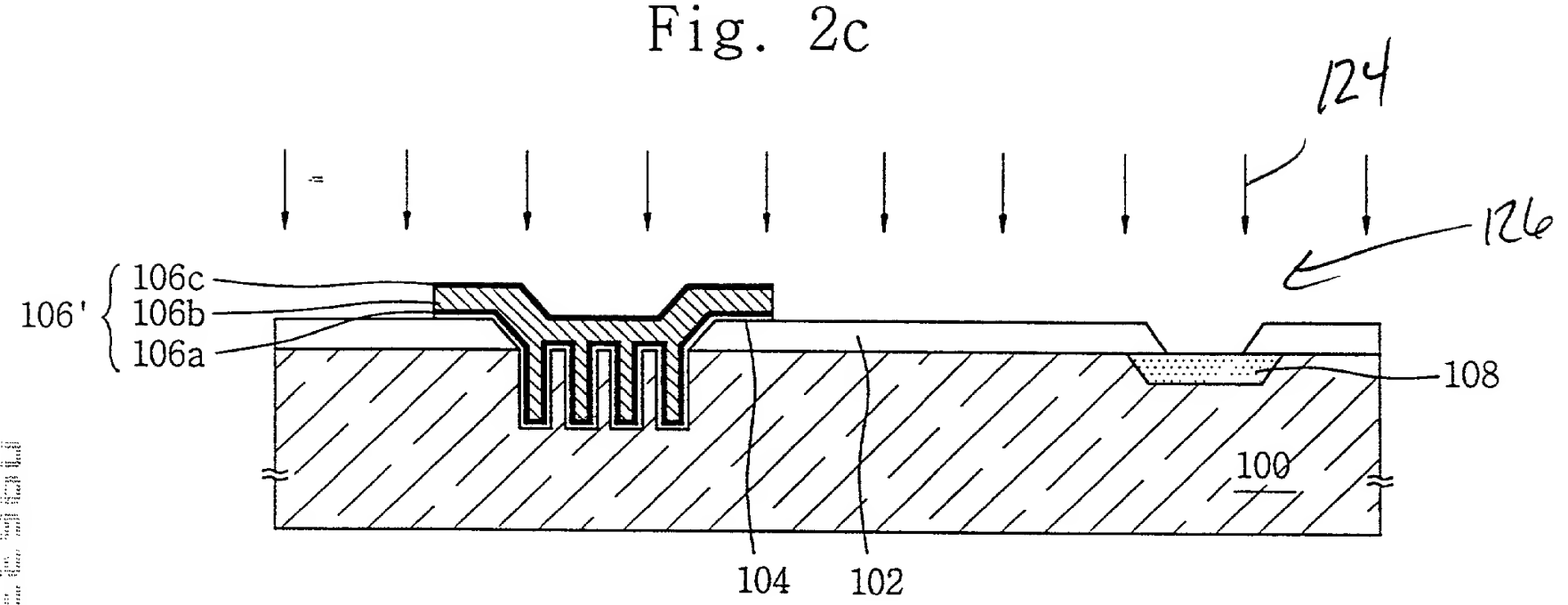
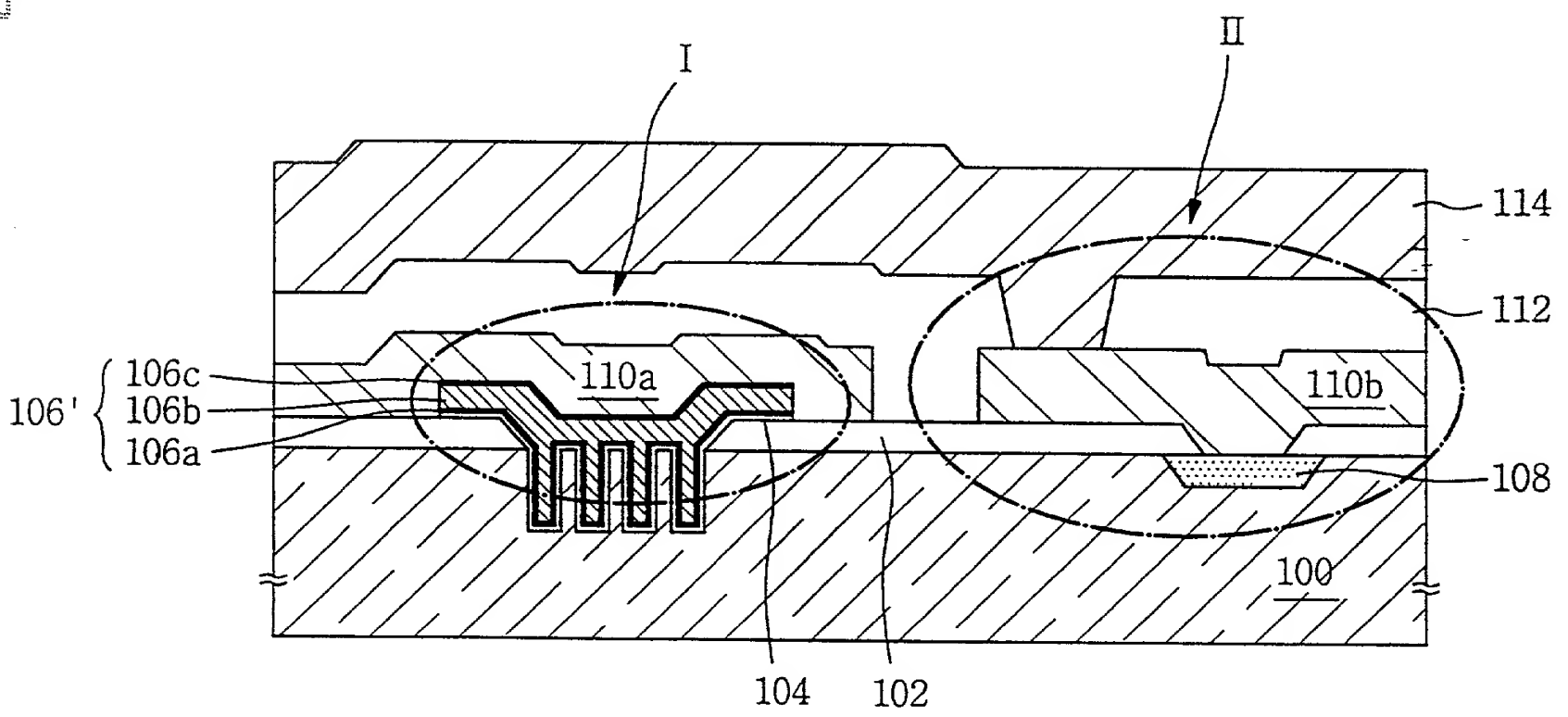

124
126
106'
106c
106b
106a
108
100
104
102

Fig. 2d


I
II
114
112
106'
106c
106b
106a
110a
110b
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DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: **SAM-126**

As a below named inventor, I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name,

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

CAPACITOR AND FABRICATING METHOD THEREFOR

the specification of which (check only one):

__X__ is attached hereto.

_____ was filed as United States Patent Application

Serial No. _____

on _____

and was amended

on _____.

(if applicable)

_____ was filed as PCT Patent Application

Serial No. _____

on _____

and was amended under PCT Article 19

on _____.

(if applicable)

I hereby state that I have reviewed and understand the contents of the specification, including the claims as amended by any amendment referred to herein.

I acknowledge the duty to disclose information which is material to the examination of this application in accordance with Title 37, Code of Federal Regulations, §1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, §119 of any foreign application(s) for patent or inventor's certificate or of any PCT international application(s) designating at least one country other than the United States of America listed below and have also identified below any foreign application(s) for patent or inventor's certificate or any PCT international application(s) designating at least one country other than the United States of America filed by me on the same subject matter having a filing date before that of the application(s) of which priority is claimed:

PRIOR FOREIGN/PCT APPLICATION(S) AND ANY PRIORITY CLAIMS UNDER 35 U.S.C. § 119:

COUNTRY (if PCT indicate PCT)	APPLICATION NUMBER	DATE OF FILING (day, month, year)	PRIORITY CLAIMED UNDER 35 U.S.C. § 119 (YES/NO)
Republic of Korea	2000-280	5 January 2000	YES

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION	Attorney Docket No: **SAM-126**

I hereby claim the benefit under Title 35, United States Code, §119(e) of any United States provisional application(s) listed below.

PRIOR U.S. APPLICATIONS FOR BENEFIT UNDER 35 U.S.C. § 119(e):

APPLICATION NUMBER	FILING DATE

I hereby claim the benefit under Title 35, United States Code, § 120 of any United States application(s) or PCT international application(s) designating the United States of America that is/are listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in that/those prior application(s) in the manner provided by the first paragraph of Title 35, United States Code, § 112, I acknowledge the duty to disclose material information as defined in Title 37, Code of Federal Regulations, § 1.56 which occurred between the filing date of the prior applications and the national or PCT international filing date of this application:

PRIOR U.S. APPLICATIONS OR PCT INTERNATIONAL APPLICATION(S) DESIGNATING THE U.S. FOR BENEFIT UNDER 35 U.S.C. § 120:

APPLICATION NUMBER (if PCT indicate PCT)	DATE OF FILING (day, month, year)	STATUS: (PATENTED, PENDING OR ABANDONED)

POWER OF ATTORNEY: As a named inventor, I hereby appoint the following attorneys and/or agents to prosecute this application and transact all business in the Patent and Trademark Office connected therewith.

Maurice E. Gauthier	Reg. No. 20,798	Patrick J. O'Shea	Reg. No. 35,305
Richard L. Stevens	Reg. No. 24,445	Arlene J. Powers	Reg. No. 35,985
Matthew E. Connors	Reg. No. 33,298	Steven M. Mills	Reg. No. 36,610
William E. Hilton	Reg. No. 35,192	Anthony P. Onello, Jr.	Reg. No. 38,572

Send Correspondence to:	Direct Telephone Calls to:
Steven M. Mills, Esq. Samuels, Gauthier & Stevens LLP 225 Franklin Street Boston, Massachusetts 02110	Steven M. Mills, Esq. (617) 426-9180 Ext. 149 (617) 426-2275 (facsimile)

Wherefore I petition that letters patent be granted to me for the invention or discovery described and claimed in the attached specification and claims, and hereby subscribe my name to said specification and claims and to the foregoing declaration, power of attorney, and this petition.

I hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

Signature	Date 2000. 7. 19

Full Name of 1st Inventor	Family Name **Lee**	First Given Name **In-Jung**	Second Given Name
Residence & Citizenship	City **Seoul**	State or Foreign Country **Republic of Korea**	Country of Citizenship **Republic of Korea**
Post Office Address	Post Office Address **497-4, Oksu 1-dong, Songdong-gu**	City **Seoul**	State & Zip Code/Country **Republic of Korea**

DECLARATION, PETITION AND POWER OF ATTORNEY FOR PATENT APPLICATION			Attorney Docket No: **SAM-126**
Signature	HEON JONG, SHIN	Date	19-JULY-2000
Full Name of 2nd Inventor	Family Name **Shin**	First Given Name **Heon-Joung**	Second Given Name
Residence & Citizenship	City **Yongin-city, Kyonggi-do**	State or Foreign Country **Republic of Korea**	Country of Citizenship **Republic of Korea**
Post Office Address	Post Office Address **#106-507, Pyuksan Apt., 99, Sanghyon-ri, Suji-eup**	City **Yongin-city, Kyonggi-do**	State & Zip Code/Country **Republic of Korea**